

**Please Amend the following claims:**

- 1    **1.** (Amended) An improved infrared transceiver system comprising:
- 2           first sensing means for detecting infrared signals incident thereon and converting
- 3    said signals to an electrical current signal;
- 4           gain control means for amplifying said current signals;[ and]
- 5           voltage conversion means for converting said current signals into voltage signals;
- 6    and
- 7           staged current amplification means in circuit between said gain control means and
- 8    said voltage conversion means, said staged amplification means comprised of at least two
- 9    amplification stages, each said stage amplifying said current signals.
- 1    **4.** (Amended) The system of Claim [2]1, wherein said gain control means comprises a
- 2    current mirror in operative connection with [a transimpedence]said staged current
- 3    amplification means[ amplifier].
- 1    **5.** (Amended) The system of Claim 4, wherein said [transimpedence amplifier]current
- 2    amplification means comprises:
- 3    a first transistor means, said first transistor means comprising a first drain and a first gate;
- 4    a second transistor means, said second transistor means comprising a second source and a
- 5    second drain, said second source being in circuit with said first drain;
- 6    a third transistor means, said third transistor means comprising a third gate and a third
- 7    source, said third gate being in circuit with said second drain; and
- 8    a fourth transistor means, said fourth transistor means comprising a fourth drain and a
- 9    fourth gate, said fourth drain in circuit with said fourth gate and said first gate.
- 1    **9.** (Amended) A improved method for detecting and amplifying incident wireless
- 2    signals, said method being implemented in a infrared transceiver system comprising

3 signal detecting means and signal amplifying means, said method comprising the steps  
4 of:

5 said signal detecting means converting said incident wireless signals into electrical  
6 current signals; and

7 said amplifying means amplifying said electrical current signals, said amplifying step  
8 comprising at least two stages of amplification of said current signals.

1 **10.** (Amended) The method of Claim 9, wherein each said stage of said amplifying  
2 comprises amplifying said current signals in a transistor operating in the weak inversion  
3 range[ gain control means further comprises staged current amplification means for  
4 amplifying said current signals in stages, said current amplification means in circuit  
5 before said voltage conversion means].

1 **11.** (Amended) An improved wireless signal receiver system, comprising:  
2 first sensing means for detecting wireless signals incident thereon and converting said  
3 signals to an electrical current signal;  
4 gain control means for amplifying said current signals, said gain control means  
5 comprising at least one transistor means operating in the weak inversion range; and  
6 voltage conversion means for converting said amplified current signals into voltage  
7 signals.

1 **12.** (Amended) The system of Claim 11, wherein said gain control means further  
2 comprises[ing] staged current amplifier[cation means] operating in the weak inversion  
3 range[in circuit between said gain control means and said voltage conversion means, said  
4 staged amplification means configured to amplify said current signals].

1 13. (Amended) The system of Claim 12, wherein said gain control means further  
2 comprises a current mirror in operative connection with [a transimpedance amplifier]said  
3 current amplifier.

1 14. (Amended) The system of Claim 13, wherein said [transimpedance ]current amplifier  
2 comprises:

3 a first transistor means, said first transistor means comprising a first drain and a first gate;

4 a second transistor means, said second transistor means comprising a second source and a  
5 second drain, said second source being in circuit with said first drain;

6 a third transistor means, said third transistor means comprising a third gate and a third  
7 source, said third gate being in circuit with said second drain; and

8 a fourth transistor means, said fourth transistor means comprising a fourth drain and a  
9 fourth gate, said fourth drain in circuit with said fourth gate and said first gate.

✓  
Please add the following new claims: ✓

B1  
1 ~~18. The system of Claim 1, wherein each said amplification stage comprises one transistor~~  
2 ~~means, each said transistor means comprising a bias voltage, and wherein said bias voltage is~~  
3 ~~dynamically adjusted in order to operate each said transistor in a weak inversion range.~~

4

**Clean Version of Amended Claims:**

B1

1 1. ~~An improved infrared transceiver system comprising:~~  
2 first sensing means for detecting infrared signals incident thereon and converting  
3 said signals to an electrical current signal;  
4 gain control means for amplifying said current signals;  
5 voltage conversion means for converting said current signals into voltage signals;  
6 and  
7 staged current amplification means in circuit between said gain control means and  
8 said voltage conversion means, said staged amplification means comprised of at least two  
9 ~~amplification stages, each said stage amplifying said current signals.~~

1 4. ~~The system of Claim 1, wherein said gain control means comprises a current mirror in~~  
2 ~~operative connection with said staged current amplification means.~~

B2  
Sub  
C1

1 5. ~~The system of Claim 4, wherein said current amplification means comprises:~~  
2 a first transistor means, said first transistor means comprising a first drain and a first gate;  
3 a second transistor means, said second transistor means comprising a second source and a  
4 second drain, said second source being in circuit with said first drain;  
5 a third transistor means, said third transistor means comprising a third gate and a third  
6 source, said third gate being in circuit with said second drain; and  
7 a fourth transistor means, said fourth transistor means comprising a fourth drain and a  
8 ~~fourth gate, said fourth drain in circuit with said fourth gate and said first gate.~~

Sub  
D17  
BB

1 9. ~~A improved method for detecting and amplifying incident wireless signals, said~~  
2 ~~method being implemented in a infrared transceiver system comprising signal detecting~~  
3 ~~means and signal amplifying means, said method comprising the steps of:~~  
4 ~~said signal detecting means converting said incident wireless signals into electrical~~  
5 ~~current signals; and~~

6 said amplifying means ~~amplifying said electrical current signals, said amplifying step~~  
7 comprising at least two stages of amplification of said current signals.

1 ~~10. The method of Claim 9, wherein each said stage of said amplifying comprises~~  
2 ~~amplifying said current signals in a transistor operating in the weak inversion range.~~

1 ~~11. An improved wireless signal receiver system, comprising:~~

2 first sensing means for detecting wireless signals incident thereon and converting said  
3 signals to an electrical current signal;

4 gain control means for amplifying said current signals, said gain control means  
5 comprising at least one transistor means operating in the weak inversion range; and

6 voltage conversion means for converting said amplified current signals into voltage  
7 signals.

1 12. The system of Claim 11, wherein said gain control means further comprises staged  
2 current amplifier operating in the weak inversion range.

1 13. The system of Claim 12, wherein said gain control means further comprises a current  
2 ~~mirror in operative connection with said current amplifier.~~

- Sub  
C3  
B3  
Cont
- 1 14. The system of Claim 13, wherein said current amplifier comprises:  
2 a first transistor means, said first transistor means comprising a first drain and a first gate;  
3 a second transistor means, said second transistor means comprising a second source and a  
4 second drain, said second source being in circuit with said first drain;  
5 a third transistor means, said third transistor means comprising a third gate and a third  
6 source, said third gate being in circuit with said second drain; and  
7 a fourth transistor means, said fourth transistor means comprising a fourth drain and a  
8 fourth gate, said fourth drain in circuit with said fourth gate and said first gate.
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